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(54) **Capacitive voltage dropper**

(57) A power supply for energizing a load such as a low-voltage incandescent lamp 11 has a main capacitor C1 in series with the load across the A.C. line source, and an auxiliary capacitor C2 connected across the main capacitor by a switching device 14 during a selected portion of the source waveform cycle. The minimum load current is established by the capacitor C1, with additional load current flowing through the capacitor C2 during those portions of the source waveform cycle when connected, whereby the load current may be adjusted over a range established by the magnitude of the main and auxiliary capacitors. The switching device 14 comprises an FET S and a parallel diode D. Control logic 16 monitors the voltages across the lamp 11 and across the capacitor C1 and turns FET S on when the voltages across the capacitors C1, C2 are substantially equal, i.e. during conduction of diode D or at a positive peak of the main capacitor voltag V_1 if diode D is non-conductive. Lamp brightness depends on how long FET S is conductive in each AC cycle and this is determined by manual or feedback adjustment of a monostable (38), (Fig. 1*h*), in control 16.

FIG. 1

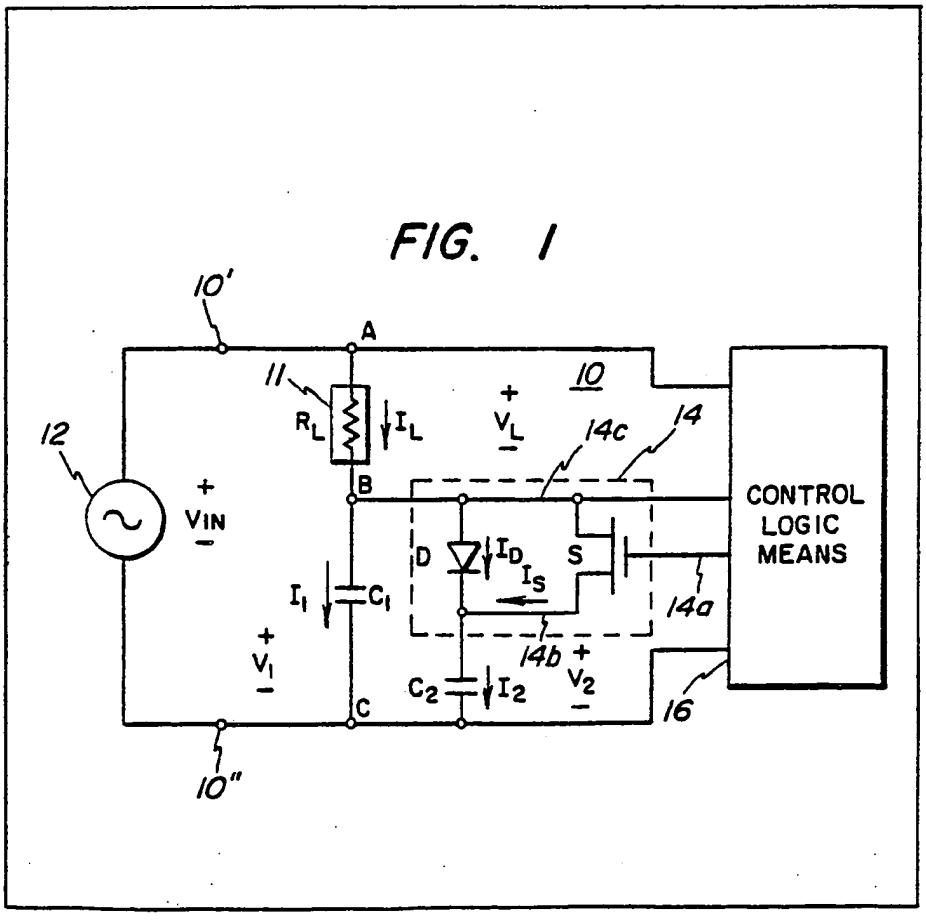

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FIG. 1

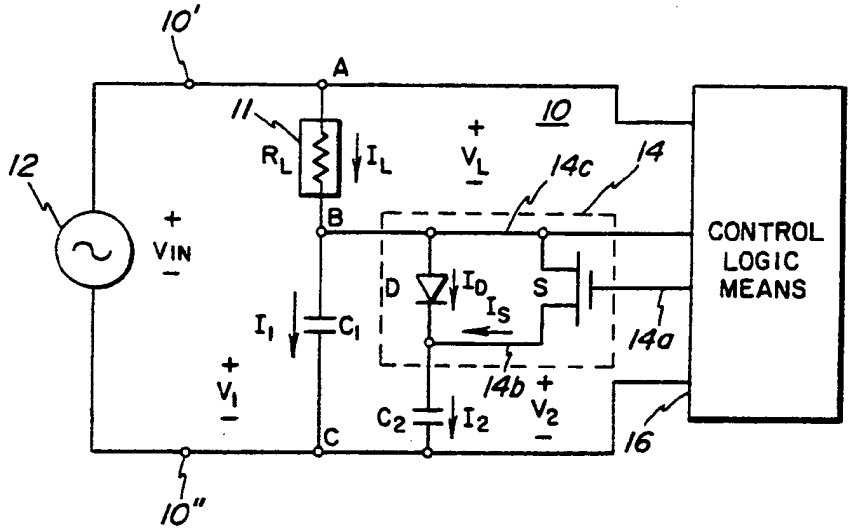
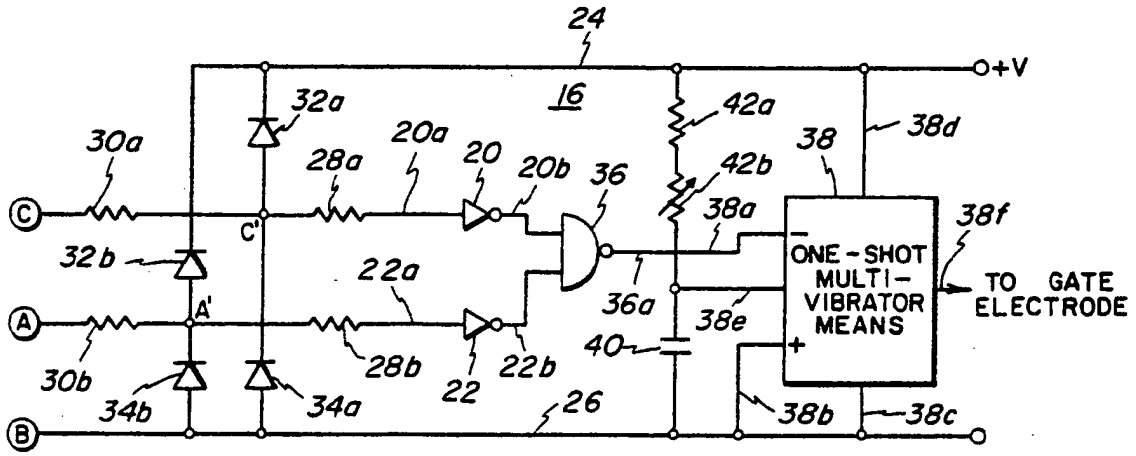

10'
A
11
10
12
R_L
I_L
V_L
14c
14
B
CONTROL LOGIC MEANS
V_{IN}
D
I_D
S
I_S
I_1
C_1
14a
14b
V_1
C_2
I_2
V_2
C
16
10"

FIG. 1h


24
16
+V
32a
30a
20a
28a
20
20b
36
42a
38
38d
42b
C
C'
38a
38f
32b
22a
ONE-SHOT MULTI-VIBRATOR MEANS
TO GATE ELECTRODE
A
A'
36a
38e
40
30b
28b
22
22b
34b
34a
26
38b
38c
B

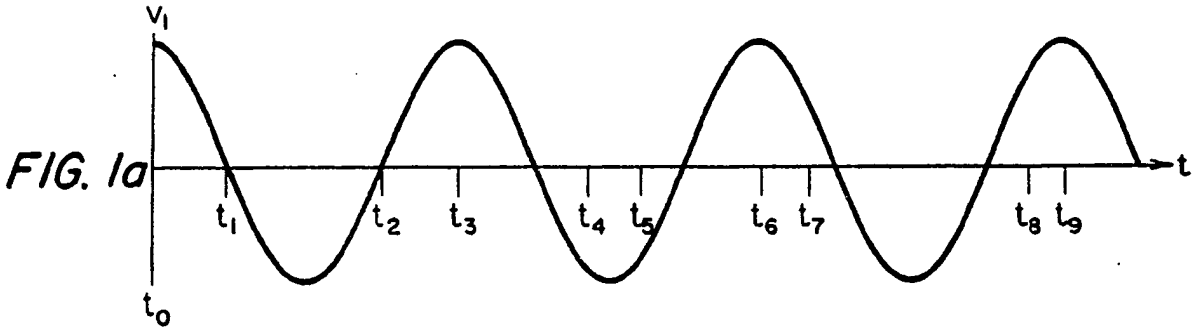


FIG. 1a

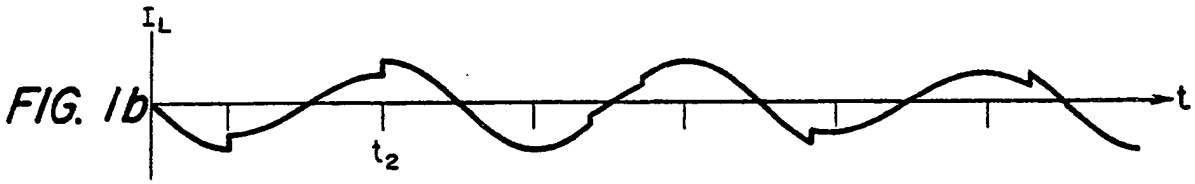


FIG. 1b

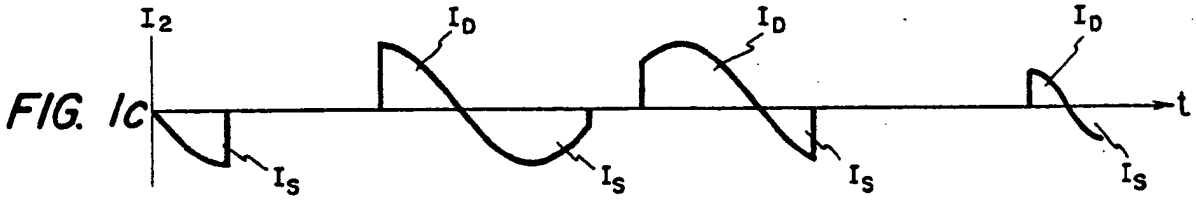


FIG. 1c

FIG. 1d

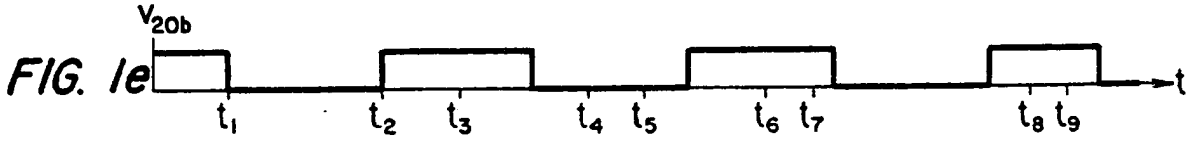


FIG. 1e

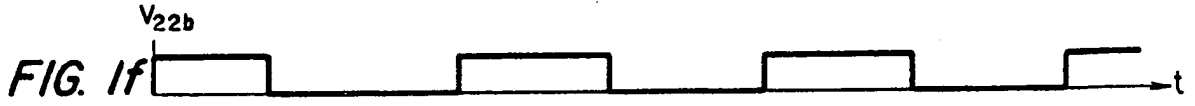


FIG. 1f

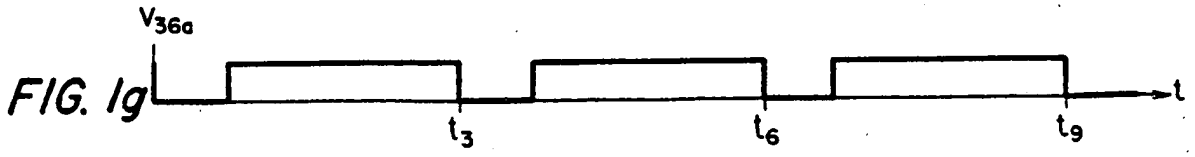


FIG. 1g

SPECIFICATION

P wer supplies for incandescent lamps

The present invention relates to low-voltage power supplies and, more particularly, to a lin - frequency power supply for energizing a low-voltage load such as an incandescent lamp.

It is often desirable to operate a low-voltage load from a relatively higher voltage A.C. source. In particular, there exists a class of low-voltage lamps having an improved efficacy due to operation of the lamp filament at a lower voltage than has been traditionally used for lamp operation. Many circuits for providing such operation either exhibit undesirably high levels of electromagnetic interference or require components having relatively high current and/or voltage ratings. In particular, previous attempts at providing low voltage power sources for incandescent lamps having utilized magnetic components for voltage transformation purposes. The cost of such magnetic components has prevented the resulting power supplies from being economical. Other power supplies have utilized phase-control waveforms, in which very narrow pulses are required, with high surge currents being provided across the load; reliability is frequently reduced in this manner. It is therefore highly desirable to provide a power supply for a low-voltage incandescent lamp and the like load, having relatively low cost, high reliability and in which components of relatively small current rating can be utilized.

In one embodiment of the invention, apparatus for supplying line-frequency current to a low-voltage load from a higher voltage A.C. source, includes a main capacitor in series with the load across the source, and an auxiliary capacitor connected across the main capacitor by a switching device for a selected portion of each source waveform cycle, responsive to a control signal provided by control logic means. A diode is connected to conduct in shunt with, and for opposite conduction polarity to, the control conduction path of the switching device. The total variation of load current is controlled by the ratio of the main capacitor value to the total capacitance (the sum of the auxiliary and main capacitor values) in the circuit. The switching device is preferably switched to its conductive condition either when the shunting diode is conductive or at a positive peak voltage across the main capacitor, if the shunting diode is nonconductive.

The control logic means preferably monitors the voltage across the main capacitor and across the load, to determine the time instant for triggering a monostable multivibrator which turns on the device for a time interval set by the multivibrator utput-puls control.

In the accompanying drawings, by way of example only:—

Figure 1 is a schematic block diagram of low-voltage load power supply embodying the present invention;

Figures 1a, 1b, 1c, 1d, 1e, 1f and 1g are time-coordinated graphical representations of the main capacitor voltage, load current, auxiliary capacitor current, switching device drive signal and intermediate control logic means voltages for illustrative load currents over the total adjustment range of the supply, and useful in understanding the principles of the present invention; and

Figure 1h is a schematic diagram of a control logic means utilizable in the circuit of Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to Figures 1, 1a, 1b, 1c and 1d the novel power supply 10 is utilized for controlling the magnitude of power applied to a load 11 from an A.C. Source 12. Load 11 can be a low-voltage incandescent lamp, for example, operating at a voltage V_L of between about 24 volts and about 36 volts. The power supply 10 enables the lamp to operate at a selectable fixed output power in a relatively small range of brightness; in such application, a relatively small range of lamp voltage V_L is required, while the lamp current I_L is variable over a predetermined e.g. about 20%, range.

Source 12 is connected to a pair of power supply terminals 10′ and 10″, respectively connected to circuit nodes A and C. The load (lamp) 11 is connected between node A and a circuit common node B. A first capacitive element, hereinafter the main capacitor, C_1 is connected between nodes B and C. Switching means 14 is connected between node B and one terminal of a second capacitive element, hereinafter the auxiliary capacitor, C_2. The remaining terminal of auxiliary capacitor C_2 is connected to node C. Terminals A, B and C, as well as the switching means control input 14a, are connected to a logic control means 16. Switching means 14 may be any device capable of controllably providing a low resistance path, between node B and that terminal of auxiliary capacitor C_2 furthest from node C, responsive to a signal at its control input 14a, such that a current can flow toward or away from the auxiliary capacitor with respect to common node B. In a preferred embodiment, switching means 14 comprises a unipolar switching device, in parallel with a diode D, having the anode thereof connected to node B and the cathode thereof connected to the auxiliary capacitor C_2. Advantageously, the switching means 14 is a power MOS field-effect transistor (MOSFET) S in which diode D is formed as a parasitic device between the drain electrode 14b and the source electrode 14c thereof.

Power supply 10 forms a dynamic parallel-switched capacitive voltage converter in which the minimum current I_L flowing through the load resistance R_L is the main capacitor current I_1. An additional component of load current I_L is due to the current I_2 flowing through auxiliary capacitor C_2. Thus, minimum load current and power occurs if current do s not flow through auxiliary capacitor C_2 at any p int during a cycle of the source 12

waveform. Conversely, maximum load current and power occurs if the auxiliary capacitor current I_2 flows for an entire source waveform cycle. A median magnitude of load current and power (and load lamp brightness) is obtained if the auxiliary capacitor current I_2 flows for approximately one-half the source waveform cycle. Thus, by changing the percentage of a source waveform cycle during which auxiliary capacitor current I_2 flows, the load current and power are adjusted. Switching device S is an active turn-off device, allowing conduction of current therethrough to be actively terminated some time after the device has been turned on. The interval between power switching device S turn-on and turn-off establishes the load current and power magnitude within the adjustment ranges thereof. To prevent undue stress on switching device S, it is desirable to control the switching of auxiliary capacitor C_2 such that circulating current is not allowed to flow between auxiliary capacitor C_2 and main capacitor C_1. Therefore, control logic means 16 is utilized to turn "on" power switching device S for conduction when the voltages V_1 and V_2 across the pair of capacitors are substantially equal, i.e. during conduction of diode D, or at a positive peak of the main capacitor voltage V_1, if diode D is non-conductive.

The operation of circuit 10 may be best understood by consideration of the main capacitor voltage V_1 and auxiliary capacitor current I_2 waveforms, in the median, substantially-maximum and substantially-minimum load current conditions. At some time t_0, the main capacitor voltage V_1 (Figure 1a) is at a positive peak and the main capacitor current I_1, because of the low power factor, is substantially 90° out-of-phase with voltage V_1, or substantially at zero magnitude. Switching device S is turned on, at time t_0, by application of an appropriate voltage V_{14a} to gate electrode 14a, with regard to common node B, by control logic means 16 (Figure 1c). The switching device S remains conductive until time t_1. In this time interval, from time t_0 to time t_1, the current through auxiliary capacitor C_2 begins to decrease toward a negative-polarity peak, which is reached at time t_1 (Figure 1b). The auxiliary capacitor current I_s flows from capacitor C_2, through the "on" channel of device S (from drain electrode 14b to source electrode 14c,) and adds to the instantaneous main capacitor current I_1 then flowing (toward load 11). Thus, the load current $I_L = I_1 + I_2$.

At time t_1, the gate electrode drive terminates, device S is turned off and current I_2 ceases to flow. The auxiliary capacitor C_2 voltage V_2 has discharged substantially to z ro volts, although the main capacitor C_1 voltage V_2 continues to decrease toward a negativ peak, as the line voltage V_{IN} approaches a negative p ak value. Thereafter, voltage V_1 begins to increase until a zero crossing is reached at time t_2. During the time interval from time t_1 to time t_2, diode D is reverse-biased and device S is turned off, whereby only the main capacitor current I_1 flows through the load 11. Thus, $I_L = I_1$ is this interval.

At time t_2, the main capacitor voltage V_1 becomes positive and greater than the substantially zero voltage remaining on auxiliary capacitor C_2; diode D becomes forward-biased and diode current I_D flows through auxiliary capacitor C_2, the diode and load 11. Thus, during the time interval between time t_2, when voltage V_1 crosses the zero axis, and time t_3, when voltage V_1 attains a peak positive value, the diode conducts and the additional current I_D flows as auxiliary capacitor current I_2, whereby the load current $I_L = I_1 + I_2$. At time t_3, the diode current is essentially zero, and diode conduction ceases. It will thus be seen that in the single-cycle time interval between time t_0 and time t_3, auxiliary capacitor current I_2 flows, in phase with main capacitor current I_1, for one-half of the cycle, establishing a median load current value.

In the substantially-maximum load current condition, illustrated for the single-cycle time interval between time t_3 and time t_6, the auxiliary capacitor current I_2 flows for the majority of the cycle (and flows for the entire cycle at the maximum load current condition). Thus, auxiliary capacitor current I_2 is caused to flow, starting at time t_3, by applying the switching device S driving waveform (Figure 1c), until turn-off time t_4. Therefore, at time t_3, device S is rendered conductive at the main capacitor voltage V_1 peak (substantially corresponding to the main capacitor current I_1 being of zero magnitude). As the main capacitor voltage V_1 decreases toward a negative peak, the main capacitor current I_1 also decreases toward a negative peak value, attained at the zero crossing of voltage V_1 in the t_3-t_4 interval, and then increases. The auxiliary capacitor current I_2 also decreases toward a negative peak and thereafter increases until time t_4, at which time the switching device is turned off and the switching device current I_S (essentially equal to the auxiliary capacitor current I_2) ceases. There is no current surge through switching device S at turn-on or turn-off, as the voltages across the capacitors are equal. At time t_4, the voltage across auxiliary capacitance C_2 is at a relatively high negative value, which is more positive than the main capacitor voltage V_1 in the time interval t_4-t_5; diode D is reverse-biased. At time t_5, the main capacitor voltage V_1 again becomes more positive than the auxiliary capacitor voltage V_2 and diode D conducts. Diode current I_D increases, until the main capacitor voltage V_1 passes through the positive-going zero crossing in time interval t_5-t_6, and thereafter decreases. The diode current I_D reaches essentially zero magnitude at t_6, when th capacitor voltage reaches a positive peak value, and diode D ceases to conduct. Therefore, the load current I_L is the sum of th in-phase main and auxiliary capacitor currents I_1 and I_2, in the time intervals t_3-t_4 and t_5-t_6; the load current is equal to the main capacitor current I_1 only in the relatively small time interval t_4-t_5. As the auxiliary capacitor current I_2 flows for a longer portion of the cycle in time interval t_3-t_6 than in time interval t_0-t_3, it will

be seen that greater load current (and therefore greater load power and load lamp brightness) occurs during the latter time interval.

In the substantially-minimum load current case, illustrated in the time interval t_6-t_9, the switching device S is again turned on while the main capacitor voltage is at a peak, at time t_6, and is only kept on for a relatively short time, being turned off at time t_7. Therefore, the auxiliary capacitor current I_2 flows through switching device S (as device current I_S) only in the relatively short time interval t_6-t_7. At time t_7, when device S is turned off, a relatively high positive voltage V_2 remains across auxiliary capacitor C_2. As main capacitor voltage V_1 decreases thereafter, diode D is reverse-biased and neither the diode nor the switching device conduct, until time t_8. At time t_8, the main capacitor voltage V_1 again reaches a positive voltage equal to the positive voltage left across the auxiliary capacitor, and diode D conducts until the end of the cycle, at time t_9, when the diode current falls to zero and diode D is about to become reverse biased. It will be seen that the load current I_L, in the time interval t_6-t_9, is equal to the sum of the in-phase main and auxiliary capacitor currents I_1 and I_2 in the time intervals t_6-t_7 and t_8-t_9, and is equal only to the main capacitor current I_1 in the time interval t_7-t_8, which forms the major portion of time interval t_6-t_9. As the time intervals t_6-t_7 and t_8-t_9 become progressively smaller, the load current also becomes progressively smaller, reaching the minimum load current, established by the main capacitor current I_1, when these time intervals become essentially zero.

It will now be seen that the total adjustment range of the load current I_L is established by the relative contribution of auxiliary capacitor current I_2 and the portion of each cycle during which that current I_2 flows, with respect to the main capacitor current I_1. By suitable choice of the capacitance of capacitor C_2, with respect to the capacitance of main capacitor C_1, the total range of load current variation is established.

Referring now to all of the Figures, and particularly Figure 1h, control logic means 16 provides the switching device S gate electrode 14a drive signal to turn on the switching device during the conduction interval of diode D or at the positive peak voltage on main capacitor C_1 if diode D is not immediately-previously conducting current. Control logic means 16 also turns off switching device S with the proper timing to establish the total load current magnitude. Circuit 16 includes first and second inverters 20 and 22, each having an input 20a or 22a respectively coupled through first and second resistance elements 28a and 30a, or 28b and 30b, to the associated one of the respective C and A nodes of the power supply. Limiting diodes 32a and 34a are connected to the junction C' between resistances 28a and 30a, and limiting diodes 32b and 34b are connected to the junction A' between resistances 28b and 30b, to limit, commonly referred to in the art as hard limit, the junctions C' and A' voltages, respectively, to be never less than one diode drop below the common node B potential and never greater than one diode drop above a positive voltage logic supply raid 24 (which voltage can be provided by known techniques). The inverter outputs 20b and 22b are each connected to a different one of the pair of inputs of a NAND gate 36. The output 36a of gate 36 is connected to the negative-going trigger input 38a of a one-shot multivibrator means 38, which may be provided as an integrated circuit monostable multivibrator. The positive-going trigger input 38b and the common supply input 38c of means 38 are connected to common node B, while the positive supply input 38d is connected to positive voltage rail 24. An output-pulse time-duration-establishing input 38e is connected to a timing capacitor 40, having the remaining terminal thereof connected to common node B, and also to positive supply rail 24 through the series-connected combination of a first, fixed timing resistance 42a and a variable timing resistance 42b. The multivibrator means output 38f is connected to the switching device input 14a, e.g. to the gate electrode of the power MOSFET device S. The value of fixed resistance 42a is selected to provide a minimum "on" time for the switching device S, and to limit the maximum current drawn by multivibrator means input 38e. The resistance magnitude of variable resistor 42b is selected to achieve a maximum "on" time for the switching device, dependent upon the ratio of maximum to minimum load current/power/brightness required.

In operation, control logic means 16 provides an open-loop control means, in which the voltage across main capacitor C_1 is sensed by the hard-limiting inverting means formed by inverter 20, resistances 28a and 30a, and limiting diodes 32a and 34a. As the main capacitor voltage V_1 becomes positive, the inverter output 20b falls from a high to a low voltage. Conversely, as V_1 becomes negative, the inverter output 20b rises from a low to a high voltage. Thus, output 20b has a low output level for positive voltages across the main capacitor and a high output level for main capacitor negative voltages. Second inverter 22, in association with resistances 28b and 30b and diodes 32b and 34b, also forms a hard-limiting inverting means sensing the voltage V_L across load 11. Therefore, the state of second inverter output 22b is an inverse measure of the load current I_L. The voltage output of 20b and 22b are shown in Figures 1d and 1e respectively. As shown in Figure 1f, the output 36a of the NAND gate will have a negatively-going transition at the peak of the main capacitor voltage. This negative-going transition triggers one-shot multivibrator means 38, to produce the positive-going gate electrode signal V_{14a}, with respect to common node B, having a time duration determined by the magnitude of capacitance 40 and the total resistance of the series-connected resistors 42a and 42b.

While control logic means 16 is shown as an

open-loop means, wherein the load current/power/brightness is established by manual adjustment of a variable resistance 42b, it should be understood that a closed-loop control logic means may be equally as well utilized, with a feedback signal being applied, as a current into capacitor 40 or a voltage into charging resistors 42a and 42b, to the monostable multivibrator to vary the conduction time interval of switching device S.

While the present invention has been described with respect to one presently preferred embodiment thereof, many variations or modifications will now become apparent to those skilled in the art. It is our intent, therefore, to be limited only by the scope of the appending claims and not by the specific details and instrumentalities described by way of example herein.

CLAIMS

1. A power supply for energizing a load at a voltage magnitude less than the voltage magnitude provided by an A.C. source, comprising:

a first reactive element in series connection with said load across said source, said first reactive element having a reactance selected to cause a minimum desired current flow through said load;

a second reactive element;

a single active switching device having a path controlled, responsive to a control signal, to connect said second reactive element in parallel connection across said first reactive element to allow current flow in a first of two directions with respect to said second reactive element; and

a unidirectionally-conducting element in parallel with the controlled path of said switching device and poled to conduct current in the remaining one of two directions with respect to said second reactive element; wherein conduction of said switching device and said unidirectionally-conductive element establishes a total load current by variation of a portion of the source waveform cycle during which an additional current flows through said second reactive element and said load.

2. The power supply of claim 1, wherein said power supply further includes a control circuit for causing said switching device to begin current conduction when the unidirectionally-conducting element is conductive or the voltage across said first reactive element is substantially at a polarity peak.

3. The power supply of claim 2, wherein the control circuit triggers said switching to begin current conduction when the voltage across said first reactive element is substantially at a positive polarity peak.

4. The power supply of claims 1 or 2, wherein said first reactive element is a first capacitive element.

5. The power supply of claim 4, wherein said second reactive element is a second capacitive element.

6. The power supply of claim 5, wherein the capacitance of said second capacitive element is less than the capacitance of said first capacitive element.

7. The power supply of claim 6, wherein the ratio of the first and second capacitive elements is selected to provide a desired range of load current variation.

8. The power supply of claim 7, wherein the load current variation range is about 20%.

9. The power supply of claim 5, wherein said control circuit provides said control signal to cause said switching device to conduct current for a controlled time interval occurring once each source waveform cycle.

10. The power supply of claim 9, wherein said control signal begins at a substantial voltage polarity peak across said first reactive element.

11. The power supply of claim 9, wherein said switching device is a metal-oxide-semiconductor field-effect transistor (MOSFET) having a current-conductive path controlled by the control signal at a gate electrode; and said unidirectionally-conducting element is a parasitic diode formed in parallel with the controlled current-conductive path of said MOSFET.

12. The power supply of claim 9, wherein said switching device conducts for a first time interval during each source waveform cycle; and wherein said unidirectionally-conducting element conducts for a second time interval, different from the first time interval, during the same source waveform cycle.

13. The power supply of claim 12, wherein said first and second time interval are of substantially equal duration.

14. The power supply of claim 13, wherein said first means includes a monostable multivibrator having an output providing a variable duration control signal to cause said switching device to conduct, responsive to a trigger signal.

15. The power supply of claim 14, wherein a signal, responsive to the current flowing through said load, varies the output duration of said monostable multivibrator.

16. The power supply of claim 14, wherein said control circuit further includes means, monitoring at least one of the voltages across said load and the voltage across said first reactive element, for providing the trigger to said monostable multivibrator.

17. The power supply of claim 9, wherein said control circuit includes first means for causing said switching device to conduct during a first time interval occurring substantially at a first positive-polarity voltage peak at the commencement of a source waveform cycle; and said unidirectionally-conducting element conducts during a second time int rval occurring before the next positive-polarity voltage peak which occurs at the end of the same source waveform cycle.

18. The power supply of claim 17, wherein said first and second time intervals are of substantially equal duration.

19. The power supply of claim 18, wherein said first means includes a monostable multivibrator having an output providing a variable duration control signal to cause said switching device to conduct, responsive to a trigger signal.

20. The power supply of claim 19, wherein a signal responsive to the current flowing through said load, varies the output duration of said monostable multivibrator.

21. The power supply of claim 19, wherein said control circuit further includes means, monitoring at least one of the voltages across said load and the voltage across said first reactive element, for providing the trigger to said monostable multivibrator.

22. The power supply of claim 17, wherein said load is an incandescent lamp.

23. The power supply of claim 2, wherein said control circuit provides said control signal to cause said switching device to conduct current for a controlled time interval occurring once each source waveform cycle.

24. The power supply of claim 23, wherein said control signal begins at a substantial voltage polarity peak across said first reactive element.

25. The power supply of claim 23, wherein said switching device is a metal-oxide-semiconductor field-effect transistor (MOSFET) having a current-conductive path controlled by the control signal at a gate electrode; and said unidirectionally-conducting element is a parasitic diode formed in parallel with the controlled current-conductive path of said MOSFET.

26. The power supply of claim 23, wherein said switching device conducts for a first time interval during each source waveform cycle; and wherein said unidirectionally-conducting element conducts for a second time interval, different from the first time interval, during the same source waveform cycle.

27. The power supply of claim 26, wherein said first and second time intervals are of substantially equal duration.

28. The power supply of claim 27, wherein said first means includes a monostable multivibrator having an output providing a variable duration control signal to cause said switching device to conduct, responsive to a trigger signal.

29. The power supply of claim 28, wherein a signal, responsive to the current flowing through said load, varies the output duration of said monostable multivibrator.

30. The power supply of claim 28, wherein said control circuit further includes means, monitoring at least one of the voltages across said load and the voltage across said first reactive element, for providing the trigger to said monostable multivibrator.

31. The power supply of claim 23, wherein said control circuit includes first means for causing said switching device to conduct during a first time interval occurring substantially at a first positive-polarity voltage peak at the commencement of a source waveform cycle; and said unidirectionally-conducting element conducts during a second time interval occurring before the next positive-polarity voltage peak which occurs at the end of that same source waveform cycle.

32. The power supply of claim 31, wherein said first and second time intervals are of substantially equal duration.

33. The power supply of claim 32, wherein said first means includes a monostable multivibrator having an output providing a variable duration control signal to cause said switching device to conduct, responsive to a trigger signal.

34. The power supply of claim 33, wherein a signal, responsive to the current flowing through said load, varies the output duration of said monostable multivibrator.

35. The power supply of claim 33, wherein said control circuit further includes means, monitoring at least one of the voltages across said load and the voltage across said first reactive element, for providing the trigger to said monostable multivibrator.

36. The power supply of claim 1, wherein said load is an incandescent lamp.

37. A power supply substantially as herein described with reference to the accompanying drawings.

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